signal line pair **101** in a multi-drop manner to simultaneously transmit a differential signal pair of EPI data to N number of source drive ICs.

[0089] FIG. **8** is a waveform view illustrating an EPI protocol for transmitting EPI data between the timing controller (TCON) and the source driver ICs SIC#**1** to SIC#**4**. FIG. **9** is a view illustrating a bit stream of a clock training pattern signal, control data, and pixel data.

[0090] Referring to FIGS. **8** and **9**, the timing controller TCON transmits a clock training pattern signal CT having a predetermined frequency to the source driver ICs SIC#**1** to SIC#**4** during a first step (phase-I) period, and when a high level lock signal LOCK is input through the lock line **102**, the timing controller TCON transitions to a second step (phase-II) signal transmission. During the second step (phase-II) period, the timing controller TCON transmits the control data CTR to the source driver ICs SIC#**1** to SIC#**4**, and when the lock signal LOCK is maintained at a high level, the timing controller TCON transitions to a third step (phase-III) signal transmission to transmit pixel data (RGB data) of an input image to the source driver ICs SIC#**1** to SIC#**4**.

[0091] In the second step (phase-II), the timing controller TCON may code a code defining entry of the bonding resistance measurement mode in a start packet of the control data. Also, in the third step (phase-III), the timing controller TCON may code it in a start packet of transmitted data. Thus, in the present disclosure, the resistance measurement mode and the measurement range may be automatically controlled using the proposed EPI protocol.

[0092] FIG. **10** is a flow chart illustrating a method for measuring contact resistance of a display device according to an embodiment of the present disclosure.

[0093] Referring to FIG. **10**, during the first step (phase-I), the timing controller TCON transmits the clock training pattern signal CT to the source driver ICs SIC#**1** to SIC#**4**, and when a lock state of DLL (LOCK=high) is input through the lock line **102**, the timing controller TCON transitions to the second step (phase-II) signal transmission. During the second step (phase-II), the timing controller TCON may select entry of resistance measurement mode (S**1** to S**3**). The source driver ICs SIC#**1** to SIC#**4** decodes a start packet of the control data to operate in the resistance measurement mode. (S**4** to S**6**). The timing controller TCON does not code the code defining the resistance measurement mode in the control data and codes a normal operation code to control the source driver ICs SIC#**1** to SIC#**4** in the normal operation mode for displaying an input image (S**7**).

[0094] As mentioned above, it should be appreciated that the method for measuring contact resistance of the present disclosure is not applied only to the source driver ICs SIC#**1** to SIC#**4**. For example, the present disclosure may be applied to a driving circuit or a flexible circuit board adhered to a substrate of a display panel through an ACF.

[0095] As mentioned above, in the present disclosure, bonding resistance between the driving circuit (or the flexible circuit board) and the display panel may be automatically measured without having to dispose a separate dummy pad on the substrate of the display panel.

[0096] In addition, in the present disclosure, rather than determining bonding resistance simply by any one of a good product level and a defective level, a resistance value thereof may be measured by differentiating the bonding resistance by a preset resistance range using the circuit illustrated in FIG. **4**.

[0097] Furthermore, since the present disclosure is implemented using the internal circuit of the drive IC, it may be implemented without burdening an additional circuit or without increasing a chip size, and since a separate dummy pad is not provided on the substrate of the display panel, a problem of static electricity introduced to the display panel through the dummy panel may be prevented. Also, since bonding resistance is automatically measured in the display panel having a narrow bezel, the present disclosure may be applied to display panel structures of various shapes.

[0098] The various embodiments described above can be combined to provide further embodiments. All of the U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet. are incorporated herein by reference, in their entirety. Aspects of the embodiments can be modified, if necessary to employ concepts of the various patents, applications and publications to provide yet further embodiments.

[0099] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

What is claimed is:

1. A display device having a circuit connected thereto, the display device comprising:

a plurality of dummy bumps disposed on the circuit;

a display panel;

shorting pads disposed on the display panel to connect dummy pads; and

a comparison circuit comparing an input voltage that is input through bonding resistance between the dummy bumps and the shorting pads with a variable reference voltage to provide a measure the bonding resistance between the circuit and the display panel.

2. The display device of claim **1**, wherein the comparison circuit changes the variable reference voltage by changing a resistance value of a dividing circuit using a plurality of resistors and a plurality of switches.

3. The display device of claim **1**, wherein the comparison circuit comprises:

a comparator having a non-inverting input terminal to which the input voltage is input, an inverting input terminal to which the variable reference voltage is input, and an output terminal from which an output signal is output;

a plurality of dividing circuits connected to the non-inverting terminal of the comparator; and

a plurality of switches connected to the dividing circuits to select a resistance value of the dividing circuits, respectively.